CLAIMS

What is claimed is:

1. A charge coupled device (CCD) image detector comprising:

an image area of an array of rows of gates, each gate of said image area array being operative to collect and store a charge content representative of a picture element (pixel) of an image, said rows of gates of the image area being operative concurrently by a first clock signal to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in a predetermined direction through said image area;

a storage area of an array of rows of gates, each gate of said storage area array being operative to store a charge content, said rows of gates of the storage area being operative concurrently by a second clock signal to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in the predetermined direction through said storage area, said storage area array of rows disposed in said CCD detector such that a first row of said image area array of rows is adjacent a last row of said storage area array of rows to accommodate a transfer in parallel of the charge contents of the gates of said first row of the image area to the gates of said last row of the storage area, wherein the image and storage areas are operative by the first and second clock signals, respectively, to transfer the charge contents of the rows of the image area array to rows of the storage area array;

a buffer area of an array of rows of gates, each gate of said buffer area array being operative to store a charge content, said rows of gates of the buffer area being operative concurrently by a third clock signal to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in the predetermined direction through said buffer area, said buffer area array of rows disposed in said CCD detector such that a first row of said storage area array of rows is adjacent a last row of said buffer area array of rows to accommodate a transfer in parallel of the charge contents of the gates of said first row of the storage area to the gates of said last row of the buffer area, wherein the storage and buffer areas are operative by the second and third clock signals, respectively, to transfer the charge contents of the rows of the storage area array to rows of the buffer area array; and

a readout register of a row of gates, each gate of said readout register being operative to store a charge content, said readout register disposed in said CCD detector such that a first row of said buffer area array of rows is adjacent the row of said readout register to accommodate a transfer in parallel of the charge contents of the gates of said first row of the buffer area to the gates of said readout register as controlled solely by the third clock signal, said row of gates of the readout register being operative concurrently by a fourth clock signal

to transfer serially the charge contents of the gates thereof through said register in a predetermined direction to an output signal line.

2. The CCD image detector of claim 1 wherein the number of rows of the image area array is equal to the composite number of rows of the storage area array and buffer area array.

3. The CCD image detector of claim 1 wherein the number of rows of the buffer area array is equal to the square root of the number of rows of the image area array rounded up to the nearest integer value.

4. The CCD image detector of claim 1 wherein the number of rows of the buffer area array is equal to the number of a designated band of rows of the image area array.

5. The CCD image detector of claim 1 comprising a timing controller for controlling the operation of the first, second, third and fourth clock signals.

6. The CCD image detector of claim 5 wherein the timing controller operates the first, second, third and fourth clock signals in a predetermined sequence to purge the CCD image detector of charge contents.

7. The CCD image detector of claim 5 wherein the timing controller operates the first, second, third and fourth clock signals in a predetermined sequence to effect a readout of the charge content of a plurality of bands of rows of gates.

8. The CCD image detector of claim 5 wherein the timing controller operates the first, second, third and fourth clock signals in a predetermined sequence to effect a readout of the charge content of an image frame.

9. The CCD image detector of claim 5 wherein timing controller is operative to: (1) control the first, second and third clock signals concurrently to transfer the charge contents of the rows of the image area array to rows of the storage area array and the buffer area array, (2) control the second and third clock signals concurrently to transfer the charge contents of the rows of the storage area array to rows of the buffer area array, (3) control the third clock signal to transfer in parallel the charge contents of the last row of the buffer area to the

readout register, and (4) control the fourth clock signal to transfer serially the charge contents of the gates of the readout register through the register in a predetermined direction to the output signal line.

10. The CCD image detector of claim 5 wherein the timing controller controls solely the third clock signal to transfer the charge contents of the buffer area array of rows to the read out register.

11. Method of operating a charge coupled device (CCD) as an image detector comprising the steps of:

(a) collecting and storing charge content in gates of an image area array of rows of gates for a predetermined period of time, said charge content of said gates of said image area array representative of a picture elements (pixels) of an image frame;

(b) transferring the stored charge contents of the image area array to a storage area array of rows of gates controlled by a burst of first clock pulses wherein each said pulse controls the transfers in parallel of the stored charge contents of gates between adjacent rows through the image and storage areas in a predetermined direction;

(c) transferring the charge contents of a predetermined number of adjacent rows of the storage area array to a like number of adjacent rows of a buffer area array of rows of gates controlled by a burst of second clock pulses wherein each said pulse controls the transfers in parallel of the stored charge contents of gates between adjacent rows through the storage and buffer areas in the predetermined direction;

(d) transferring in parallel the charge contents of adjacent rows through the buffer area array in the predetermined direction by a pulse of a third clock so that the charge contents of a last row of gates of the buffer area array are transferred in parallel to a row of gates in a readout register;

(e) shifting out the charge contents of the gates of the readout register serially to an output of the CCD as controlled by the pulses of a fourth clock;

(f) thereafter, repeating steps (d) and (e) for each row of the predetermined number of adjacent rows of stored charge content of the buffer area array transferred from the storage area array in step (d); and

(g) repeating steps (c)-(f) for each predetermined number of adjacent rows of a set of predetermined number of adjacent rows of the storage area array.

12. The method of claim 11 including the steps of:

(h) dividing the storage area array into a plurality of bands of rows wherein each band of said plurality includes a predetermined number of adjacent rows of charge content; performing step (c) until a first band of charge content of said plurality of bands is transferred to the buffer area array;

(j) performing steps (d) through (f) in sequence until the charge content of the buffer area array is shifted to the output of the CCD;

(k) performing step (c) until another band of charge content of said plurality of bands is transferred to the buffer area array; and

(l) repeating steps (j) and (k) in sequence until all of the bands of charge content of said plurality are shifted to the output of the CCD.

13. The method of claim 12 wherein the storage area array is divided into a plurality of mutually exclusive bands.

14. The method of claim 12 including the steps of: setting equal the predetermined number of rows of each band of the plurality of bands; and setting the number of rows of the buffer area array equal to the predetermined number of rows of each band.

15. The method of claim 11 including the steps of:

(h) dividing the entire storage area array into a plurality of adjacent bands of rows wherein each band of said plurality includes a predetermined number of adjacent rows of charge content;

(i) performing step (c) until a first band of charge content of said plurality of bands is transferred to the buffer area array;

(j) performing steps (d) through (f) in sequence until the charge content of the buffer area array is shifted to the output of the CCD;

(k) performing step (c) until another band of charge content of said plurality of bands is transferred to the buffer area array; and

(l) repeating steps (j) and (k) in sequence until all of the bands of charge content of the storage area array are shifted to the output of the CCD.

16. The method of claim 15 wherein the entire storage area of 512 rows is divided into 16 adjacent bands of 32 rows each.

17. The method of claim 15 including the step of optimizing substantially the number of rows of the buffer area array to minimize the number of times step (d) is repeated.

18. The method of claim 15 including the step of setting the number of rows of the buffer area array equal to the square root of the number of rows of the image area array rounded up to the next highest integer.

19. The method of claim 11 including the step of purging the charge contents from the gates of the rows of the CCD prior to the execution of step (a).

20. The method of claim 11 including the step of repeating steps of (a) through (g) periodically.